

IN THE CLAIMS:

Claims 1-29 have been amended herein. All of the pending claims 1 through 29 are presented below. This listing of claims will replace all prior versions and listings in the application. Please enter these claims as amended.

1. (Currently Amended) A method for forming a semiconductor device assembly, comprising:

providing a carrier substrate including at least one die-attach location and at least one terminal

adjacent to saidthe at least one die-attach location; and

providing a solder mask on saidthe carrier substrate, saidthe solder mask including at least one device-securing region positioned over at least a portion of saidthe at least one die-attach location, at least one recessed area adjacent to saidthe at least one device-securing region, and at least one dam adjacent to saidthe at least one recessed area, opposite from saidthe at least one device-securing region, saidthe at least one dam contacting at least a portion of a peripheral edge of saidthe at least one terminal.

2. (Currently Amended) The method of claim 1, further comprising:

applying adhesive material to at least one of saidthe at least one device-securing region of saidthe solder mask and a bottom surface of at least one semiconductor device to be secured to saidthe at least one device-securing region.

3. (Currently Amended) The method of claim 2, further comprising:

positioning saidthe at least one semiconductor device to on saidthe at least one device-securing region, saidthe adhesive material located between saidthe bottom surface and saidthe at least one device-securing region securing saidthe at least one semiconductor device to saidthe at least one device-securing region.

4. (Currently Amended) The method of claim 3, wherein said positioning comprises applying force to at least one of saidthe at least one semiconductor device and saidthe carrier substrate.

5. (Currently Amended) The method of claim 3, wherein said positioning comprises forcing saidthe adhesive material to spread between saidthe bottom surface of saidthe at least one semiconductor device and saidthe at least one device-securing region.

6. (Currently Amended) The method of claim 5, wherein said positioning comprises causing excess adhesive material to flow laterally beyond at least one of a peripheral edge of saidthe at least one semiconductor device and a periphery of saidthe at least one device-securing region.

7. (Currently Amended) The method of claim 6, further comprising: receiving saidthe excess adhesive material within saidthe at least one recessed area.

8. (Currently Amended) The method of claim 6, wherein saidthe at least one dam prevents saidthe excess adhesive material from contaminating a connection surface of saidthe at least one terminal.

9. (Currently Amended) The method of claim 1, wherein said-providing saidthe solder mask comprises providing a solder mask with saidthe at least one dam comprising a laterally extending portion configured to cover at least portion of a peripheral edge of a connection surface of saidthe at least one terminal.

10. (Currently Amended) The method of claim 1, wherein said-providing saidthe solder mask comprises providing saidthe carrier substrate with saidthe solder mask already secured thereto.

11. (Currently Amended) The method of claim 1, wherein ~~said~~ providing ~~said~~the solder mask includes securing a preformed solder mask to a surface of ~~said~~the carrier substrate.

12. (Currently Amended) The method of claim 1, wherein ~~said~~ providing ~~said~~the solder mask includes forming ~~said~~the solder mask on a surface of ~~said~~the carrier substrate.

13. (Currently Amended) The method of claim 12, wherein ~~said~~ forming is effected stereolithographically.

14. (Currently Amended) The method of claim 12, wherein ~~said~~ forming comprises forming a plurality of at least partially superimposed, contiguous, mutually adhered material layers.

15. (Currently Amended) A method ~~for a~~ for designing ~~solder~~ a solder mask for use on a carrier substrate, comprising:

configuring at least one device-securing region to have a semiconductor device secured thereto;
and

configuring a plurality of raised dams to be positioned adjacent to and in contact with peripheries of terminals of the carrier substrate.

16. (Currently Amended) The method of claim 15, further comprising:
configuring at least one recessed area between at least a portion of a periphery of ~~said~~the at least one device-securing region and at least one of ~~said~~the plurality of raised dams.

17. (Currently Amended) A method for designing a solder mask for use on a carrier substrate, comprising:

configuring at least one device-securing region to have a semiconductor device secured thereto;

and

configuring at least one recessed area adjacent to said the at least one device-securing region.

18. (Currently Amended) The method of claim 17, further comprising:

configuring a plurality of raised dams adjacent to said the at least one recessed area, opposite

from said the at least one device-securing region.

19. (Currently Amended) A method for designing a solder mask to be used on a carrier substrate, comprising:

configuring at least one device-securing region of the solder mask to be located over at least a portion of a die-attach location of the carrier substrate;

configuring at least one recessed area laterally adjacent to said the at least one device-securing region; and

configuring at least one dam adjacent to said the at least one recessed area, opposite from said the at least one device-securing region, to be located laterally adjacent to and contact a peripheral edge of a terminal protruding from a surface of the carrier substrate, and to have a height at least as great as a height of said the at least one device-securing region.

20. (Currently Amended) The method of claim 19, wherein said-configuring said the at least one dam comprises configuring said the at least one dam to include a laterally extending ledge positionable over at least a portion of a peripheral edge of a connection surface of the terminal.

21. (Currently Amended) The method of claim 19, wherein ~~said~~-configuring ~~said~~the at least one dam comprises configuring ~~said~~the at least one dam to have a height that exceeds ~~said~~the height of ~~said~~the at least one device-securing region.

22. (Currently Amended) The method of claim 21, wherein ~~said~~-configuring ~~said~~the at least one dam comprises configuring ~~said~~the at least one dam to be located at an elevation which is substantially the same as or less than an elevation of an active surface of a semiconductor device to be positioned on ~~said~~the at least one device-securing region.

23. (Currently Amended) A method for designing a carrier substrate, comprising: configuring a substantially planar substrate to include at least one die-attach location; and configuring at least one terminal adjacent to ~~said~~the at least one die-attach location and to protrude a sufficient distance from ~~said~~the substantially planar substrate to prevent excess adhesive material forced from between a semiconductor device and ~~said~~the at least one die-attach location from contaminating a connection surface of ~~said~~the at least one terminal.

24. (Currently Amended) The method of claim 23, further comprising: configuring an adhesive-receiving area between ~~said~~the at least one die-attach location and ~~said~~the at least one terminal.

25. (Currently Amended) The method of claim 24, wherein ~~said~~-configuring ~~said~~the adhesive-receiving area comprises configuring at least one recess.

26. (Currently Amended) The method of claim 25, wherein ~~said~~-configuring at least one recess comprises configuring ~~said~~the at least one recess to substantially laterally surround ~~said~~the at least one die-attach location.

27. (Currently Amended) The method of claim 25, wherein ~~said~~ configuring at least one recess comprises configuring ~~said~~the at least one recess to be located adjacent to only a portion of ~~said~~the at least one die-attach location.

28. (Currently Amended) The method of claim 23, wherein ~~said~~ configuring ~~said~~the at least one terminal comprises configuring ~~said~~the at least one terminal to have a height that is at least as great as an elevation at which a bottom surface of the semiconductor device will be supported above a surface of ~~said~~the substantially planar substrate.

29. (Currently Amended) The method of claim 28, wherein ~~said~~ configuring ~~said~~the at least one terminal comprises configuring ~~said~~the at least one terminal to have a height that is, at most, substantially the same as an elevation at which a top surface of the semiconductor device will be located upon securing the semiconductor device relative to ~~said~~the substantially planar substrate.